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EXAMINER	
YUEN, KAN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,040	JAMES, RALPH	
	Examiner	**Art Unit**	
	Kan Yuen	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 30 March 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-44 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-44 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date See Continuation Sheet.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :3/30/2004, 11/22/2004, 1/14/2005, 4/18/2005, 4/25/2005, 7/15/2005, 8/1/2005, 8/22/2005, 2/14/2006, 6/23/2006, 3/6/2007, 4/26/2007.

Detailed Action

Note

In claim 19, line 2, the term "adapted to" is not a positive claimed limitation, because its not known whether the limitation after the term "adapted to" should be considered or not. The applicant is suggested to change or amend the term in any claims which contains the term.

Claim Objections

1. Claims 14-44 are objected to because of the following informalities:

In claim 14, line 11, 17, 22, the term "the interface" is lack of antecedent basis, because its not known whether the term is referring back to the terms "downstream reception interface", or "downstream transmission interface". Similar problem exist in claims 22, 30, 39,

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Holmberg et al. (Pat No.: 4982485).

For claim 1, Holmberg et al. disclosed the method of synchronizing an upstream and downstream link coupled to the controller (see column 2, lines 32-45, and see fig. 1); sequentially synchronizing downstream links starting with the downstream link coupled between the controller and the first hub (see column 7, lines 1-30, and see fig. 1, and fig. 2A-D). The master node 11, and a plurality of 12A-12N slave nodes are shown in fig. 1. The master node starts to sequentially synchronizing the link 13A through link 13 (N+1). We can interpret that the links from 13A through 13 (i) are the downstream links, and from link 13 (i+1) through link 13 (N+1) are the upstream links. The master node can be considered as the controller, and the slave nodes can be considered as the memory hubs; sequentially synchronizing upstream links starting with the upstream link coupled between the last memory hub and the next upstream hub (see column 7, lines 1-30, and see column 8, lines 5-25, and see fig. 1, and fig. 2A-D). The upstream synchronization is started in the link 13 (I+1) between the slave node 12 (i) and slave node 12 (i+1); providing an indication to the controller when the upstream link between the first and second hubs has been synchronized (see column 5, lines 57-67, column 6, lines 1-2, and see column 8, lines 5-25, and see fig. 1, and fig. 2A-D). Fig2 A-D shown four types of messages originated by the master node. The data transfer message shown in fig. 2D is transmitted based on the synchronization message. The data transfer message is transmit to slave node 12A, and node 12A will pass it on to the next slave node until it reaches back to the master node, which

indicates that all slaves nodes have received it; sequentially enabling downstream links to process functional commands; sequentially enabling upstream links to process functional commands, and providing an indication to the controller that all links have been enabled (see column 6, lines 35-58, see column 8, lines 49-65, and see fig. 1, and fig. 2A-D). The download network message enables the slave nodes 12 to determine their respective positions in the system; where determining their respective positions can help each node the self-configuring to adjust delay time to perform measurements in synchronism.

Regarding claim 2, Holmberg et al. also disclosed the method of synchronizing each of the links comprises applying test data signals over the links, and adjusting a phase shift of a generated receive clock signal relative to the data signals (see column 8, lines 49-65, and see fig. 1, and fig. 2A-D). The network parameter message 50 is considered as a test signal which being transmitted to the slave nodes. The signal enables the slave nodes to determine their respective position of time delay, so that it can adjust the delay time for synchronism respectively.

Claim Rejections - 35 USC § 103

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6,7 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Holmberg et al. (Pat No.: 4982485).

Regarding claim 6, Holmberg et al. also disclosed the method of synchronizing each upstream and downstream link; in a counter-clockwise order starting with the downstream link coupled between the controller and the first memory module, signaling to the next adjacent clockwise link that the prior clockwise link has been synchronized (see column 7, lines 1-30, and see fig. 1, and fig. 2A-D). The master node 11, and a plurality of 12A-12N slave nodes are shown in fig. 1. The master node starts to sequentially synchronizing the link 13A through link 13 (N+1). We can interpret that the links from 13A through 13 (i) are the downstream links, and from link 13 (i+1) through link 13 (N+1) are the upstream links. The master node can be considered as the controller, and the slave nodes can be considered as the memory hubs. When each slave node receives the synch message 60, it establish a delay time period, and then forwards the message to the next slave node. Therefore it can be interpreted as signaling to the next node that the previous link has been synchronized; detecting

through the upstream link coupled between the controller and the first memory module when all links have been synchronized (see column 5, lines 57-67, column 6, lines 1-2, and see column 8, lines 5-25, and see fig. 1, and fig. 2A-D). Fig2 A-D shown four types of messages originated by the master node. The data transfer message 70 shown in fig. 2D is transmitted based on the synchronization message. The data transfer message is transmit to slave node 12A, and node 12A will pass it on to the next slave node until it reaches back to the master node. The master node detects to receive the message 70 return back, so that it knows all slaves nodes have received it; in a counter-clockwise order starting with the downstream link coupled between the controller and the first memory module, enabling each link; and detecting through the upstream link coupled between the controller and the first memory module when all links have been enabled (see column 6, lines 35-58, see column 8, lines 49-65, and see fig. 1, and fig. 2A-D). The download network message 50 enables the slave nodes 12 to determine their respective positions in the system; where determining their respective positions can help each node the self-configuring to adjust delay time to perform measurements in synchronism. The master node waits for the network message 50 to return so that it knows all slave nodes have received this message. Although Holmberg et al. did not disclose the method of clockwise order, however it is skill in the art to either perform in counter-clock or clock order. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the obviousness in the network of Holmberg et al. The motivation for using the obviousness in the network of Holmberg being that it increases the flexibility of the network.

Regarding claim 7, Holmberg et al. also disclosed the method of synchronizing each of the links comprises applying test data signals and adjusting a phase shift of a generated receive clock signal relative to the data signals (see column 8, lines 49-65, and see fig. 1, and fig. 2A-D). The network parameter message 50 is considered as a test signal which being transmitted to the slave nodes. The signal enables the slave nodes to determine their respective position of time delay, so that it can adjust the delay time for synchronism respectively.

7. Claims 3-5, 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmberg et al. (Pat No.: 4982485), in view of Miyazaki (Pat No.: 4078228).

For claim 3, Holmberg disclosed all the subject matter of the claimed invention with the exception of inverting the test data signals and providing the inverted test data signals over the upstream link coupled to the controller. Miyazaki from the same or similar fields of endeavor teaches the method of inverting the test data signals and providing the inverted test data signals over the upstream link coupled to the controller (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Miyazaki in the network of Holmberg et al. The motivation for using the method as taught by Miyazaki in the network of Holmberg et al., being that the method enhances the balance of data distribution in the system.

Regarding claim 4, Miyazaki disclosed the method of providing an indication to the controller that all links have been enabled comprises providing an enablement command over the upstream link coupled to the controller (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;

Regarding claim 5, Miyazaki disclosed the method of the enablement command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;

Regarding claim 8, Miyazaki disclosed the method of signaling to the next adjacent clockwise link that the prior clockwise link has been synchronized comprises providing an inversion signal to next adjacent clockwise link (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413.

Regarding claim 9, Miyazaki disclosed the method of in response to the inversion signal inverted test data signals are applied over the next adjacent link (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413.

Regarding claim 10, Miyazaki disclosed the method of each link includes a transmission port and a reception port, and wherein enabling each link comprises first enabling the transmission port and thereafter enabling the reception port (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided

to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;

Regarding claim 11, Miyazaki disclosed the method of the reception port in each link is enabled by the transmission port applying an enable command to the reception port (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11).

Regarding claim 12, Miyazaki disclosed the method of the enable command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode;

Regarding claim 13, Miyazaki disclosed the method of once the reception port of a given link has been enabled, an enable signal is supplied to the transmission port of the next adjacent clockwise port to thereby enable the transmission port of the next adjacent clockwise port (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode.

8. Claims 14-18, 22-26, 30, 32-35, 39, 41,42, 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruhovets et al. (Pub No.: 20040193821), in view of Miyazaki (Pat No.: 4078228), Driskill et al. (Pat No.: 6064706), and the admitted prior.

For claim 14, Ruhovets et al. disclosed the method of memory modules, (see fig. 1, 110A-110D), and each memory modules has a downstream receiver 212,

downstream transmitter 216, upstream receiver 214, and upstream transmitter 218 shown in fig. 2. However Ruhovets et al. did not disclose the method of a downstream and upstream reception interfaces operable in an initialization mode to adjust a phase of a generated receive clock signal relative to applied test data signals and to generate an inversion signal once a final phase of the generated receive clock is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface in the normal mode of operation; a downstream and upstream transmission interfaces operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to the inversion signal from the downstream reception interface and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface into the normal mode of operation. However, the admitted prior art (see paragraph 0008, lines 1-15), disclosed the method when the controller enters a synchronization mode, the controller applies a test pattern to the memory devices, and thereafter adjusts the phase of the strobe signal. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by the admitted prior art in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by the admitted prior art in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system. Miyazaki from the same or similar fields of endeavor teaches the method of generate an inversion signal once a final phase of the

generated receive clock is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface in the normal mode of operation (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413. The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Miyazaki in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by Miyazaki in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system. Driskill et al. from the same or similar fields of endeavor teaches the method of a downstream transmission interface operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to the inversion signal from the downstream reception interface (see column 2, lines 15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24 based on the speed up signal 28, and slow down signal 30; and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface into the normal mode of operation (see column 2, lines 42-65, and see fig. 2). The write generator unit 46 generates a write enable signal 48 to storage unit 50 to allow for storing a full address of data at a location determined by a write address generator 52. Thus, it would have been

obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Driskill et al. in the downstream and upstream transmission interfaces of Ruhovets et al. The motivation for using the method as taught by Driskill et al. in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system.

Regarding claim 15, Miyazaki disclosed the method of the enablement command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode.

Regarding claim 16, Driskill et al. disclosed the method of the downstream and upstream transmission interfaces adjust the value of the corresponding test data signals responsive to the inversion signal by inverting the test data signals (see column 2, lines 15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24.

Regarding claim 17, Ruhovets et al. disclosed the method of local hub circuitry coupled to the interfaces, the local control circuitry operable process memory requests during the normal mode of operation and to develop corresponding memory signals on a memory bus output (see fig. 3, memory 224, see paragraph 0031, lines 1-15, and paragraph 0032, lines 1-15). The memory 224 can be considered as the local hub circuitry coupled to the dram interface 222. The memory 224 operate memory requests during active mode and generates signal to the data transmit circuit 226.

Regarding claim 18, Ruhovets et al. disclosed the method of memory signals comprise address, data, and control signals (see paragraph 0014, lines 1-15). The controller sends a command signal to the memory module, and the module decodes the command signal to determine if the signal intended for it. Hence, we can the control command signal has an address, and data.

Regarding claim 22, Ruhovets et al. disclosed the method of memory modules or hubs, (see fig. 1, 110A-110D), and each memory hubs has a downstream receiver 212, downstream transmitter 216, upstream receiver 214, and upstream transmitter 218 shown in fig. 2; local hub circuitry coupled to the interfaces and to the memory devices (see fig. 2). The command decode & clock recovery unit can be considered as the local hub couple to the dram interface and to buffers 212 and 216; However Ruhovets et al. did not disclose the method of a downstream and upstream reception interfaces operable in an initialization mode to adjust a phase of a generated receive clock signal relative to applied test data signals and to generate an inversion signal once a final phase of the generated receive clock is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface in the normal mode of operation; a downstream and upstream transmission interfaces operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to the inversion signal from the downstream reception interface and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface

into the normal mode of operation. However, the admitted prior art (see paragraph 0008, lines 1-15), disclosed the method when the controller enters a synchronization mode, the controller applies a test pattern to the memory devices, and thereafter adjusts the phase of the strobe signal. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by the admitted prior art in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by the admitted prior art in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system. Miyazaki from the same or similar fields of endeavor teaches the method of generate an inversion signal once a final phase of the generated receive clock is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface in the normal mode of operation (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413. The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Miyazaki in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by Miyazaki in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system. Driskill et al. from the same or similar fields of endeavor teaches the method of a downstream transmission interface operable in the initialization mode to apply test data signals on an

output and operable to adjust the value of the test data signals responsive to the inversion signal from the downstream reception interface (see column 2, lines 15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24 based on the speed up signal 28, and slow down signal 30; and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface into the normal mode of operation (see column 2, lines 42-65, and see fig. 2). The write generator unit 46 generates a write enable signal 48 to storage unit 50 to allow for storing a full address of data at a location determined by a write address generator 52. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Driskill et al. in the downstream and upstream transmission interfaces of Ruhovets et al. The motivation for using the method as taught by Driskill et al. in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system.

Regarding claim 23, Miyazaki et al. disclosed the method of the enablement command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode.

Regarding claim 24, Driskill et al. disclosed the method of the downstream and upstream transmission interfaces adjust the value of the corresponding test data signals responsive to the inversion signal by inverting the test data signals (see column 2, lines

15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24.

Regarding claim 25, Ruhovets et al. disclosed the method of the memory signals comprise address, data, and control signals (see paragraph 0014, lines 1-15). The controller sends a command signal to the memory module, and the module decodes the command signal to determine if the signal intended for it. Hence, we can the control command signal has an address, and data.

Regarding claim 26, Ruhovets et al. disclosed the method of the memory devices comprise SDRAMs (see paragraph 0022, lines 1-7).

Regarding claim 30, Ruhovets et al. disclosed the method of memory modules, (see fig. 1, 110A-110D), and each memory modules has a downstream receiver 212, downstream transmitter 216, upstream receiver 214, and upstream transmitter 218 shown in fig. 2; a plurality of memory modules coupled in series, each module being coupled to adjacent modules through respective downstream and upstream high-speed communications links (see fig. 1-2, see paragraph 0014, lines 1-15, and see paragraph 0015, lines 1-10); each memory module comprising: a plurality of memory devices (see fig. 1-2, see paragraph 0014, lines 1-15, and see paragraph 0015, lines 1-10); and local hub circuitry coupled to the interfaces and to the memory devices (see fig. 2). The command decode & clock recovery unit is the local hub couple to the dram interface and to buffers 212 and 216; and a system controller coupled to a first one of the memory modules through respective downstream and upstream high-speed communications links (see fig. 1 memory controller 104, and bus 106A). However

Ruhovets et al. did not disclose the method of a downstream and upstream reception interfaces operable in an initialization mode to adjust a phase of a generated receive clock signal relative to applied test data signals and to generate an inversion signal once a final phase of the generated receive clock is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface in the normal mode of operation; a downstream and upstream transmission interfaces operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to the inversion signal from the downstream reception interface and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface into the normal mode of operation. However, the admitted prior art (see paragraph 0008, lines 1-15), disclosed the method when the controller enters a synchronization mode, the controller applies a test pattern to the memory devices, and thereafter adjusts the phase of the strobe signal. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by the admitted prior art in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by the admitted prior art in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system. Miyazaki from the same or similar fields of endeavor teaches the method of generate an inversion signal once a final phase of the generated receive clock is determined, and operable in an enablement mode responsive to receiving an

enablement command to generate an enablement signal and to place the interface in the normal mode of operation (Miyazaki see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413. The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Miyazaki in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by Miyazaki in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system. Driskill et al. from the same or similar fields of endeavor teaches the method of a downstream transmission interface operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to the inversion signal from the downstream reception interface (see column 2, lines 15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24 based on the speed up signal 28, and slow down signal 30; and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface into the normal mode of operation (see column 2, lines 42-65, and see fig. 2). The write generator unit 46 generates a write enable signal 48 to storage unit 50 to allow for storing a full address of data at a location determined by a write address generator 52. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as

taught by Driskill et al. in the downstream and upstream transmission interfaces of Ruhovets et al. The motivation for using the method as taught by Driskill et al. in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system.

Regarding claim 32, Miyazaki disclosed the method of the enablement command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode.

Regarding claim 33, Driskill et al. disclosed the method of the downstream and upstream transmission interfaces adjust the value of the corresponding test data signals responsive to the inversion signal by inverting the test data signals (see column 2, lines 15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24.

Regarding claim 34, Ruhovets et al. disclosed the method of the memory signals comprise address, data, and control signals (see paragraph 0014, lines 1-15). The controller sends a command signal to the memory module, and the module decodes the command signal to determine if the signal intended for it. Hence, we can the control command signal has an address, and data.

Regarding claim 35, Ruhovets et al. disclosed the method of the memory devices comprise SDRAMs (see paragraph 0022, lines 1-7).

Regarding claim 39, Ruhovets et al. disclosed the method of a processor (see fig. 1, CPU 100); a system controller coupled to the processor through respective

downstream and upstream high-speed communications links (see fig. 1-2, see paragraph 0014, lines 1-15, and see paragraph 0015, lines 1-10); a plurality of memory modules coupled in series, each module being coupled to adjacent modules through respective downstream and upstream high-speed communications links, and a first one of the modules being coupled to the processor through respective downstream and upstream high-speed communications links (see fig. 1-2, see paragraph 0014, lines 1-15, and see paragraph 0015, lines 1-10). The CPU 100 is coupled to the host bridge 102, and to the first memory module 110A; each memory module comprising: a plurality of memory devices (see fig. 2, memory buffer 224); a plurality of memory modules, (see fig. 1, 110A-110D), and each memory modules has a downstream receiver 212, downstream transmitter 216, upstream receiver 214, and upstream transmitter 218 shown in fig. 2; and local hub circuitry coupled to the interfaces and to the memory devices (see fig. 2). The command decode & clock recovery unit is the local hub couple to the dram interface and to buffers 212 and 216. However Ruhovets et al. did not disclose the method of a downstream and upstream reception interfaces operable in an initialization mode to adjust a phase of a generated receive clock signal relative to applied test data signals and to generate an inversion signal once a final phase of the generated receive clock is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface in the normal mode of operation; a downstream and upstream transmission interfaces operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to the

inversion signal from the downstream reception interface and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface into the normal mode of operation. However, the admitted prior art (see paragraph 0008, lines 1-15), disclosed the method when the controller enters a synchronization mode, the controller applies a test pattern to the memory devices, and thereafter adjusts the phase of the strobe signal. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by the admitted prior art in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by the admitted prior art in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system. Miyazaki from the same or similar fields of endeavor teaches the method of generate an inversion signal once a final phase of the generated receive clock is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface in the normal mode of operation (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413. The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Miyazaki in the downstream and upstream reception interfaces of Ruhovets et al. The motivation for using the method as taught by Miyazaki in the network of Ruhovets et al.

being that it enhances the balance of data distribution in the system. Driskill et al. from the same or similar fields of endeavor teaches the method of a downstream transmission interface operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to the inversion signal from the downstream reception interface (see column 2, lines 15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24 based on the speed up signal 28, and slow down signal 30; and operable in the enablement mode responsive to the enablement signal from the downstream reception interface to provide the enablement command on the output and to place the interface into the normal mode of operation (see column 2, lines 42-65, and see fig. 2). The write generator unit 46 generates a write enable signal 48 to storage unit 50 to allow for storing a full address of data at a location determined by a write address generator 52. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Driskill et al. in the downstream and upstream transmission interfaces of Ruhovets et al. The motivation for using the method as taught by Driskill et al. in the network of Ruhovets et al. being that it enhances the balance of data distribution in the system.

Regarding claim 41, Miyazaki disclosed the method of the enablement command comprises a NOP command (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode.

Regarding claim 42, Ruhovets et al. disclosed the method of the memory devices comprise SDRAMs (see paragraph 0022, lines 1-7).

Regarding claim 44, Ruhovets et al. disclosed the method of the processor comprises a central processing unit (CPU) (see fig. 1, CPU 100).

9. Claims 19-21, 27-29, 36-38, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruhovets et al. (Pub No.: 20040193821), in view of Miyazaki (Pat No.: 4078228), Driskill et al. (Pat No.: 6064706), and the admitted prior, as applied to claim 18 above, and further in view of Komaki et al. (Pub No.: 20040160206).

For claims 19, 27, 36, 43 Ruhovets et al., Miyazaki, and Driskill et al. all disclosed the subject matter of the claimed invention with the exception of the reception interfaces include optical interfaces adapted to receive data words from an optical communications link. Komaki from the same or similar fields of endeavor teaches the method of the reception interfaces include optical interfaces adapted to receive data words from an optical communications link (see paragraph 0036, lines 1-8, and see fig. 1, and 3). Each servo is connected with the same optical link 4. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Komaki et al. in the network of Ruhovets et al. The motivation for using the method as taught by Komaki et al. in the network of Ruhovets et al. being that it increases the transmission speed.

Regarding claim 20, 28, 37 Komaki et al. disclosed the method of the downstream reception interface and the upstream transmission interface are adapted to

be coupled to the same optical communications link, and wherein the downstream transmission interface and the upstream reception interface are adapted to be coupled to the same optical communications link (see paragraph 0036, lines 1-8, and see fig. 1, and 3). Each servo is connected with the same optical link 4.

Regarding claim 21, 29, 38 Komaki et al. disclosed the method of the optical communications link comprises an optical fiber (see paragraph 0036, lines 1-8, and see fig. 1, and 3). Optical link is optical fiber.

10. Claims 31, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruhovets et al. (Pub No.: 20040193821), in view of Miyazaki (Pat No.: 4078228), Driskill et al. (Pat No.: 6064706), and the admitted prior, as applied to claim 30 above, and further in view of Park (Pat No.: 6256325).

For claims 31, 40 Driskill et al. disclosed the method of a downstream transmission interface coupled to the downstream high-speed communications link, the interface operable in the initialization mode to apply test data signals on an output and operable to adjust the value of the test data signals responsive to an inversion signal (see column 2; lines 15-40, and see fig. 1-2). The unit digital desynchronizer 10 is shown in fig. 1. The adjusted clock signal 22 is modified in the oscillator 24 based on the speed up signal 28, and slow down signal 30; and operable in the enablement mode responsive to an enablement signal to provide an enablement command on the output and to place the interface into the normal mode of operation (see column 2, lines 42-65,

and see fig. 2). The write generator unit 46 generates a write enable signal 48 to storage unit 50 to allow for storing a full address of data at a location determined by a write address generator 52. Miyazaki from the same or similar fields of endeavor teaches the method of an upstream reception interface coupled to the upstream high-speed communications link, the interface operable in the initialization mode to adjust a phase of a generated receive clock signal relative to applied test data signals and to generate the inversion signal once a final phase of the generated receive clock signal is determined, and operable in an enablement mode responsive to receiving an enablement command to generate an enablement signal and to place the interface into the normal mode of operation (see column 12, lines 57-68, and column 13, lines 1-10, and see fig. 11). In fig. 11, the inverter 412 inverted incoming signal to gate 413. The battery 416 is provided to generate an enablement signal to supplies the station shown in fig. 11 in operation or normal mode. However, Driskill et al. and Miyazaki both did not disclose the method of operable responsive to receiving the enablement command to generate a ready signal indicating all the memory modules have been synchronized. Park from the same or similar fields of endeavor teaches the method of operable responsive to receiving the enablement command to generate a ready signal indicating all the memory modules have been synchronized (see fig. 2, and see column 4, lines 40-65). The control logic generates a ready signal based on the completion of synchronization of request signal from CPU 50. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the method as taught by Park et al. in the network of Ruhovets et al., Miyazaki, Driskill et al. The motivation

for using the method as taught by Park in the network of Ruhovets et al., Miyazaki, Driskill et al. being that it increases the system reliability.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure. Baba et al. (Pat No.: 6278755), and Ellis (Pat No.: 6324485), are show systems which considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kan Yuen whose telephone number is 571-270-2413. The examiner can normally be reached on Monday-Friday 10:00a.m-3:00p.m EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky O. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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